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EXAMINER	
LEE, SIU M	

ART UNIT	PAPER NUMBER
2611	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/627,881	SAED, ARYAN	
	Examiner	Art Unit	
	Siu M. Lee	2611	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,9 and 10* is/are rejected.

7)☒ Claim(s) *3-6,8 and 11-13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *7/25/2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *10/7/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-2, 7 and 9-10 are rejected under 35 U.S.C. 102(b) as being anticipated by Wright et al. (US 6,313,703 B1).

(1) Regarding claim 1:

Wright et al. (US 6,313,703 B1) discloses a digital branch calibrator (adaptive control processing and compensation estimator 28 and digital compensation signal processor 21 and analog to digital conversion 27 in figure 3A) for use in an RF transmitter (20 in figure 3A) for compensating for phase and/or gain imbalances between two phasor fragment signals ($Ph_A(t)$ 13 and $Ph_B(t)$ 14 in figure 1 and 3A, column 9, lines 22-34) in a transmit path from a phasor fragmenter (signal component separator 11 in figure 3A, column 9, lines 21-23) in a digital front end of said transmitter (digital domain in figure 3A) to a power amplification and combining component (amplifier 15 ,16 and amplifier power combining and sampling 25 in figure 3A, column 10, lines 35-60) in an analog front end (analog domain in figure 3A) of said transmitter outputting an RF transmit signal (ks(t) 18 in figure 3A) based on a sum of said fragment signals, said calibrator comprising:

a closed loop controller (adaptive control processing and compensation estimator 28 and digital compensation signal processor 21 and analog to digital conversion 27 in figure 3A, column 11, lines 52-53) operable during a calibration sequence (training sequence when power up, column 11, lines 58-61) , defined by a predetermined number of control loop iterations (the predetermined number of loops is equal to the maximum power level divided by a predetermined increment, steps 334 and 340 in figure 27, column 39, lines 34-49), and comprising transmit and feedback signal paths (open loop real time forward data flow 31 and real time feed back loop: reverse data flow 32 in figure 3A) (column 10, lines 61-65), said transmit signal path configured for transmitting a zero base band transmit signal (antiphase training signal, column 11 line 65-column 12 line 2) and said feedback signal path configured for receiving a feedback signal correlated with a power level of said output RF transmit signal (residual output power, column 39, lines 43-44), said transmit signal path comprising a phase and/or gain adjusting component (adaptive control processing and compensation estimator 28 and digital compensation signal processor 21 in figure 3A, column 9, lines 29-34) configured for adjusting the phase and/or gain of said phasor fragment signals ($Ph_A(t)$ 13 and $Ph_B(t)$ 14 in figure 3A, column 9, lines 29-34) to minimize said power level (within a predetermined specification, column 39, lines 40-44), said adjusting being performed iteratively to the end of said calibration sequence (the transmitter is at the maximum power setting, loop between steps 334 and 340 in figure 27, column 39, lines 37-40) and resulting in sequence phase and/or gain update signals (the tap coefficients of the FIR compensation circuits in figure 10A are updated by adaptive control

processor and compensation estimator 28, column 18, lines 21-25), whereby said sequence update signals are provided for updating the phase and/or gain of data signals transmitted through said transmit signal path (estimation of correction parameter values and forms control/update signal path 34 in figure 3A, column 11, lines 37-45); and,

digital signal processing means (adaptive control processing and compensation estimator 28 and digital compensation signal processor 21 and analog to digital conversion 27 in figure 3A) (column 12, lines 37-40) configured for operating said controller and controlling said transmission of said zero base band transmit signal (control signal 29 in figure 3A, antiphase training signal generate by training signal generator 11a in figure 3A, column 12, lines 23-25) for processing by said calibrator.

(2) Regarding claim 2:

Wright et al. disclose a calibrator (adaptive control processing and compensation estimator 28 and digital compensation signal processor 21 and analog to digital conversion 27 in figure 3A) wherein said closed loop controller further comprises false imbalance removal means for removing from said feedback signal any portion thereof correlating to local oscillator and/or other non-imbalance feed through energy at the carrier frequency, said false feedback removal means comprising a digital modulator/demodulator configured for modulating said zero base band signal by a sub-carrier frequency signal (digital quadrature modulator 251 in figure 25, column 34, lines 27-30) and for demodulating said feedback signal (digital quadrature demodulator 265 in figure 26, column 35, lines 25-30).

(3) Regarding claim 7:

Wright et al. discloses an RF transmitter having a LINC architecture (column 7, lines 39-43) and comprising a digital front end (digital domain in figure 3A) with a fragmenter (signal component separator 11 in figure 3A, column 9, lines 21-23) configured for fragmenting an input signal (s(t) 12 in figure 3A) into a plurality of output fragment signals ($Ph_A(t)$ 13 and $Ph_B(t)$ 14 in figure 1 and 3A, column 9, lines 22-34) which sum to said input signal (column 9, equation 1), and an analog front end (analog domain in figure 3A) for amplification and combining of said fragment signals (amplifier 15 ,16 and amplifier power combining and sampling 25 in figure 3A, column 10, lines 35-60), said transmitter comprising a calibrator further comprising an in-phase (I), quadrature-phase (Q) signal pre-balancing component (IQPBAL) in the digital front end transmit path configured for mitigating I/Q phase and/or gain imbalances on each said fragment signal (the FIR compensation circuits 92 and 93 in figure 10A and the IQ modulator correction circuits 94 and 95 in figure 10B of the digital compensation signal processor 21) (column 18, lines 35-38, lines 63-66).

(4) Regarding claim 9:

Wright et al. discloses a method (amplifier system) for compensating for phase and/or gain imbalances between two phasor fragment signals ($Ph_A(t)$ 13 and $Ph_B(t)$ 14 in figure 1 and 3A, column 9, lines 22-34) in a transmit path (open loop real time forward data flow 31 in figure 3A) of an RF transmitter outputting an RF transmit signal (ks(t) 18 in figure 3A, column 10, lines 56-60) based on a sum of said fragment signals (s(t) 12 in figure 3A), said method comprising:

transmitting a zero base band transmit signal (antiphase training signal generate by training signal generator 11a in figure 3A, column 11 line 65-column 12 line 2) along a transmit path (open loop real time forward data flow 31 in figure 3A) during a calibration sequence (training process during power up of the transmitter, column 39, lines 34-47) defined by a predetermined number of iterations (the predetermined number of loops is equal to the maximum power level divided by a predetermined increment, steps 334 and 340 in figure 27, column 39, lines 34-49);

receiving a feedback signal (real time feed back loop: reverse data flow 32 in figure 3A) correlated with a power level of said output RF transmit signal (residual output power, column 39, lines 40-44); and,

adjusting the phase and/or gain (the update of the complex coefficients will correct the amplitude scaling and phase shift, column 17, lines 50-52) of said phasor fragment signals to minimize said power level (within a predetermined specification, column 39, lines 40-44), said adjusting being performed iteratively to the end of said calibration sequence (when the power of the transmitter is at the maximum setting, step 340 in figure 27, column 39, lines 47-49) and resulting in sequence phase and/or gain update signals (the tap coefficients of the FIR compensation circuits in figure 10A are updated by adaptive control processor and compensation estimator 28, column 18, lines 21-25), whereby said sequence update signals are provided for updating the phase and/or gain of data signals transmitted through said transmit signal path (column 18, lines 35-55, column 19, lines 4-6).

(5) Regarding claim 10:

Wright et al. discloses a method (amplifier system) as discussed above further including the step of removing from said feedback signal any portion thereof correlating to local oscillator and/or other non-imbalance feed through energy at the carrier frequency, said removing including modulating said zero base band signal by a sub-carrier frequency signal (digital quadrature modulator 251 in fig 25, column 34, lines 27-30) and demodulating (digital quadrature demodulator 265 in figure 26, column 35, lines 25-30) said feedback signal.

Allowable Subject Matter

3. Claims 3-6, 8 and 11-13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims and overcome the objections, set forth in this office action.

The following is a statement of reasons for the indication of allowable subject matter: The present invention describes a digital branch calibrator for an RF transmitter wherein the phase and/or gain adjusting component comprises a complex accumulator and a DC removal component for removing DC signal component of the feedback signal. The method for compensating the phase and/or gain imbalance is performed by alternating the iterations of phase adjustment and iterations of gain adjustment; the phase adjustment includes producing a phase gradient calculated from the magnitude of the feedback signal and the gain adjustment includes producing a gain gradient

calculated from the magnitude of the feedback signal; and the gain update signal(s) are calculated so as to limit the magnitudes of the phasor fragment signals to a predetermined maximum value L and so that the magnitude of at least one of said phasor fragment signals has the value L.

The closest prior arts, Wright et al. (US 6,313,703 B1) discloses the use of antiphase signals for predistortion training within an amplifier system. However, Wright fails to disclose the complex accumulator and a DC removal component for removing DC signal component of the feedback signal, also the method for compensating the phase and/or gain imbalance is performed by alternating the iterations of phase adjustment and iterations of gain adjustment; the phase adjustment includes producing a phase gradient calculated from the magnitude of the feedback signal and the gain adjustment includes producing a gain gradient calculated from the magnitude of the feedback signal; and the gain update signal(s) are calculated so as to limit the magnitudes of the phasor fragment signals to a predetermined maximum value L and so that the magnitude of at least one of said phasor fragment signals has the value L. The distinct features have been added to the dependent claims 3, 8, and 11-13, therefore, rendering them allowable.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Horowitz et al. (US 5,722,056) discloses a radio transmitter with power amplifier linearizer. Huang et al (US 6,885,241 B2) discloses a type-based

baseband predistorter function estimation technique for non-linear circuits. Weldon (US 6,794,938 B2) discloses a method and apparatus for cancellation of third order intermodulation distortion and other nonlinearities. Huttunen (US 7,062,233 B2) discloses a transmitter linearization. Ratto (US 6,798,844 B2) discloses a correction of phase and amplitude imbalance of I/Q modualtor. Whitemarsh et al. (US5,381,108) discloses an automatic calibration of the quadrature balance within a Cartesian amplifier. Dartois (US 6,885,709 B1) discloses a method for linearising a power amplifier over a wide frequency band. Valentine et al. (US 5,748,678) discloses a radio communication apparatus.

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Siu M. Lee whose telephone number is (571) 270-1083. The examiner can normally be reached on Mon-Fri, 7:30-4:00 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chieh Fan can be reached on (571) 272-3042. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Siu M. Lee
10/1/2006

CHIEH M. FAN
SUPERVISORY PATENT EXAMINER